Pulsed Operation and Performance of Commercial GaN HEMTs

F. Fornetti[#1], K.A. Morris[#2], M.A. Beach[#3]

[#] *Centre for Communications Research, University of Bristol, MVB, Woodland Rd, BS8 1UB, Bristol, UK*

[1]F.Fornetti@bris.ac.uk

[2]Kevin.Morris@bris.ac.uk

[3]M.A.Beach@bris.ac.uk

***Abstract*— The present study investigates the behaviour and performance of commercially available GaN HEMTs provided by Cree Inc. The gain and power variations at pulse repetition frequencies (PRFs) in the range 100-400 kHz are presented. Rise and fall times are also investigated at different PRFs and power levels. The pulsed RF waveforms are obtained by switching the gate bias of the transistor on and completely off to ensure that the device goes through full transients for every pulse. The RF frequency at which the study is conducted is 3.5 GHz.**

The aim of the study is to assess the suitability of commercial GaN HEMTs to pulsed RF applications such as Radar.

I. INTRODUCTION

GaN HEMTs have recently become a commercial reality and are an increasingly popular choice when power, linearity and robustness are required. This technology, however, is not as well understood and established as its GaAs counterpart and a number of studies have reported potential problems with devices fabricated on this material. Namely current reduction due to surface states [1-3] and buffer traps [1], virtual gate formation [2], gate and drain lag transients [4] and RF performance limitations due to non-linearities in the source resistance [5]. Most of the aforementioned studies evaluate the performance of GaN HEMTs for CW operation, however trapping effects could potentially be exacerbated by operating the device in pulsed mode. Some traps have a release time of the order of ms [1, 3] and could therefore cause a considerable current and hence power reduction.

One of the major hurdles in the development of GaN HEMTs was the reduction in channel current due to surface state traps which has been overcome by manufacturers by using SiN passivation. Solutions have also been proposed to avoid the formation of a virtual gate at high drain voltages [2] in the form of single [6-9] or double field plates [10]. Thanks to the use of field plates manufacturers have now been able to add devices to their HEMTs portfolio, that can work at higher drain voltages (typically 48 V).

The robustness and high power density of GaN HEMTs could make them the ideal replacement for vacuum tube devices currently used in a number of Radar systems.

In this paper we analyse the behaviour of commercial GaN HEMTs provided by Cree (CGH40010) when operated in pulsed mode. Such devices are passivated but they do not have field plates hence the maximum drain voltage for which they are specified is 28 V and the maximum power rating is 10W. Although this may seem a relatively low output power for a Radar application, the aim was to investigate the presence of undesirable effects which are mainly related to the structure of the device rather than its power capabilities. Higher power devices in the same range would just be a scaled up version and therefore, lower power ones may be used for these investigations without loss of generality.

The gain and power variations at Pulse Repetition Frequencies (PRFs) in the range 100-400 kHz are presented. Rise and fall times are also investigated at different PRFs and power levels. Lower PRFs, 1 kHz – 90 kHz were also investigated, however the results are not included here. The focus of this paper will be on the higher PRF range in order to analyse the performance of the devices under more demanding operating conditions.

II. TEST PROCEDURE

The 3.5 GHz pulsed RF waveforms were obtained by switching the gate bias of the transistor on and completely off to ensure that the device would go through full transients for every pulse. The PRFs ranged between 100 kHz and 400 kHz. A purpose-built interface board was used to transform TTL voltage levels generated with an Agilent 81110A into the bias levels required to switch the transistor on and off. During the on time, the bias voltage was -1.6 V and during the off time it was kept at -5 V.

Cree supplied their own test board which provided a matching network optimized for operation at 3.5 GHz and 200mA. The capacitors on the gate power rails were completely removed with the exception of the $\lambda/4$ termination capacitance.

Both gate and drain waveforms were recorded on an Agilent Infinium 54855A scope which has a 6 GHz bandwidth. The envelope of the drain signal was then recovered and smoothed using Matlab routines. The recovered envelope was then used for rise/fall time and pulse width reduction calculations.

The pulse width and rms value reduction at higher PRFs was found to be chiefly due to limitations in the interface board's ability to switch the voltage fast enough. This was confirmed when additional capacitance was removed and faster MOSFETs were used for the switching circuit. The limitation in the switching ability of the transistor may also partly be attributed to its own input capacitance.

The rise and fall times of the TTL pulses were set to 100ns to avoid spikes and glitches which may have been dangerous given the lack of safety capacitance at the gate of the HEMT. This choice also limited the switching circuit performance at higher PRFs. The gate waveforms generated by the gate bias switching circuit are shown in Fig 1.

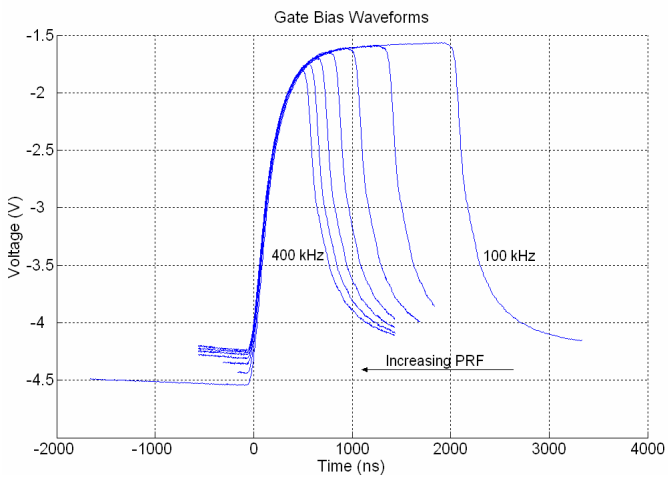

Fig 1 Bias switching waveforms as observed at the HEMT gate

The output power of the transistor was measured with an average power meter and the actual pulse power was calculated based on the true duty cycle which was derived from the actual pulse width. The gain was also adjusted to account for the reduction in pulse width and rms value caused by the bias switching circuit limitations.

III. Experimental Results

A. Power and Gain Profiles

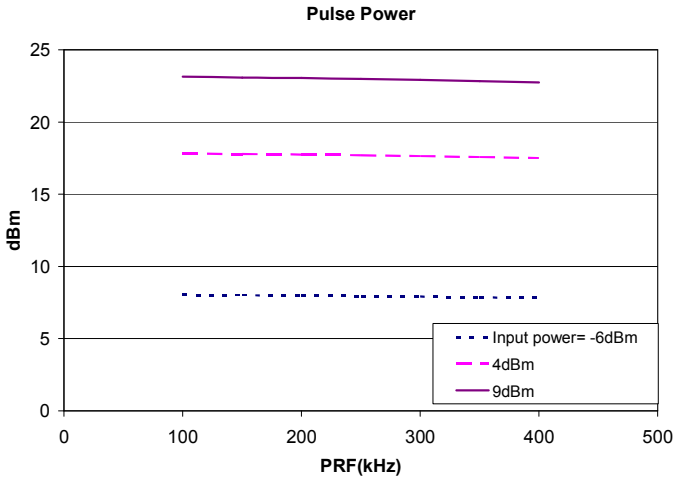

Fig 2 Pulse Power vs PRF at input powers ranging from -6 to 9 dBm

Fig 2 shows the output power variation at different input powers as the PRF is increased. It can be seen that the power remains largely constant across the PRF range. This would suggest that there is no current reduction due to trapping effects or self heating at the power levels used. As shown in Fig 3, the peak amplitude of the voltage waveforms also stays largely constant across the PRF range.

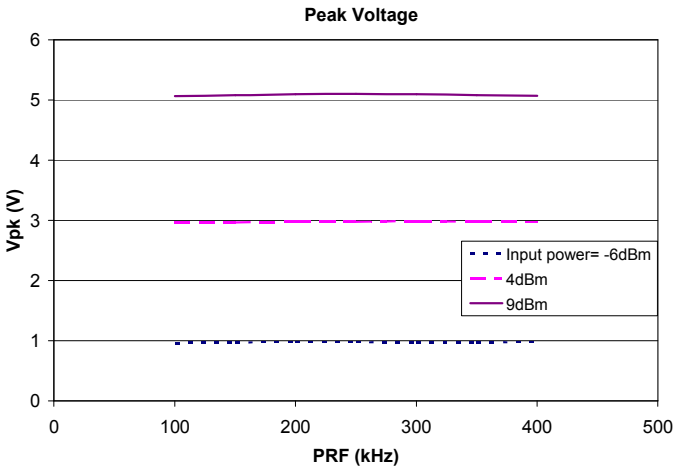

Fig 3 Peak voltage amplitude vs PRF

A slight reduction in the power gain was observed as the PRF was increased (Fig 4). The maximum gain variation observed was 0.8 dB at 9 dBm input power. However, as shown in Fig 1, this is mainly due to the changes in the gate bias waveforms which are characterised by a lower peak voltage and higher rise and fall times at higher PRFs.

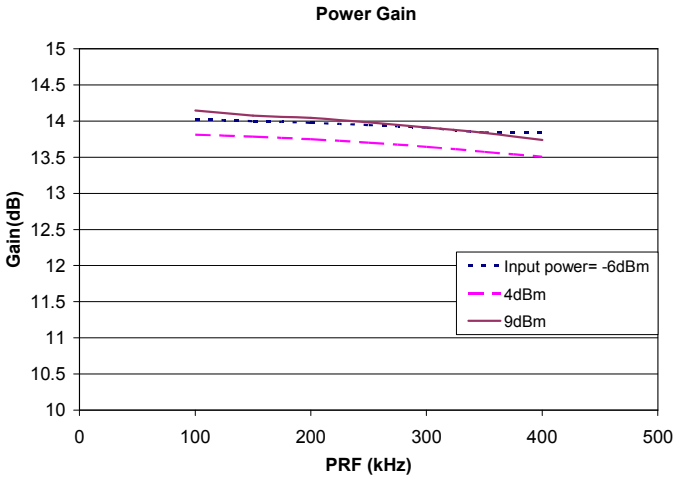

Fig 4 Power Gain vs PRF

B. Switching Times

In this section we present the changes in rise and fall times observed at the output of the HEMT.

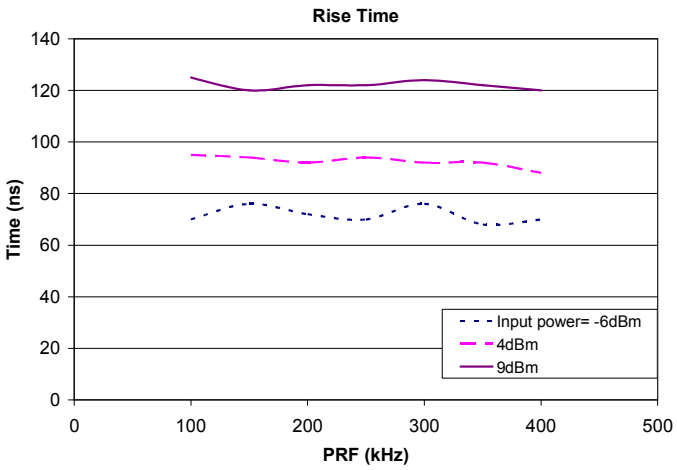

Fig 5 Rise time vs PRF

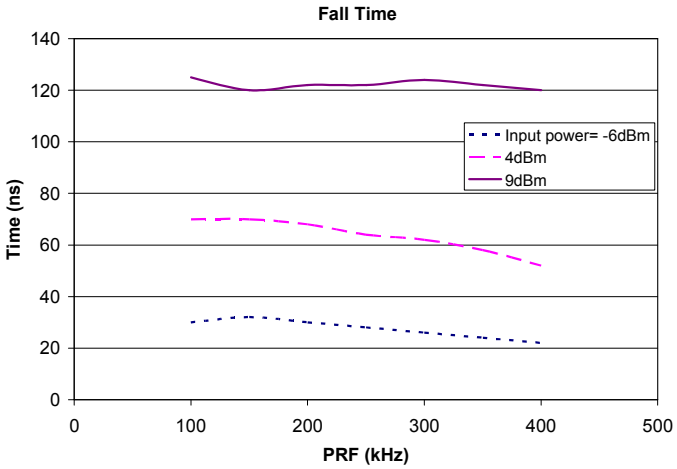

Fig 6 Fall time vs PRF

As can be seen from Fig 5 and Fig 6 the rise and fall times of the RF pulses do increase as the input power is increased. This is likely to be due to a greater capacitive load determined by higher RF voltages being present. Charge and discharge times of the capacitive elements present in the transistor package and the transistor itself increase as the input power increases.

Nevertheless, the rise and fall times show very slight changes across the PRF range for a given power level. The maximum variations observed on the rise and fall times were 8 and 18 ns respectively. It should be noted however that these values have a limited degree of accuracy due to the difference in the number of sample points available at different PRFs (lower at higher PRFs) and to the averaging preformed during data analysis. In the light of these considerations the rise and fall times can be considered constant at a given power level across the PRF range.

C. Time Waveforms

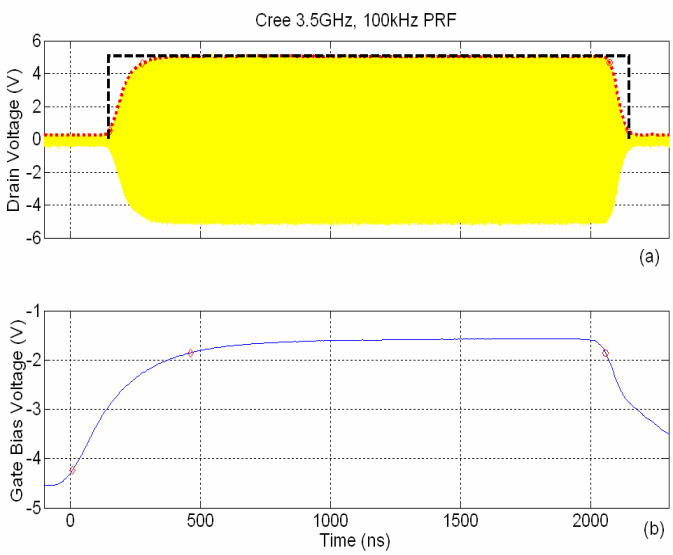

Fig 7 (a) Drain output at 9 dBm input power and 100 kHz PRF, Envelope (dotted), Ideal Envelope (dashed) – (b) Gate Bias

Fig 7 shows the gate and drain waveforms obtained at a 9 dBm input power and 100 kHz PRF. The dashed line shows the ideal envelope shape for the PRF chosen. This of course has a zero rise time which is unachievable in practice. The dotted line shows the actual envelope of the output signal.

There is a minimal pulse width reduction at 100 kHz but a finite rise and fall time which decreases slightly the rms value of the pulse.

Capacitive effects can also be seen on the gate waveform where both rising and falling slopes of the pulse are relatively low. Nevertheless the voltage excursion shown is much greater than the voltage range to which the gate of the transistor can respond. Such large rise times in the gate waveforms are therefore mitigated and can be seen to be much shorter if only the relevant bias voltage range, -2.5 V to -1.6 V, is considered.

Fig 8 shows the drain and gate voltage at a much higher PRF, 400 kHz. It is apparent that capacitive effects are much more significant at this stage and the bias voltage rise and fall times play a more prominent role. It was found during the experiments that even a few pF could make a significant difference to the actual pulse width and the rms value of the pulse. At 400 kHz such an rms value is decreased albeit to a relatively small extent. This is chiefly due to a long rise time in the gate bias.

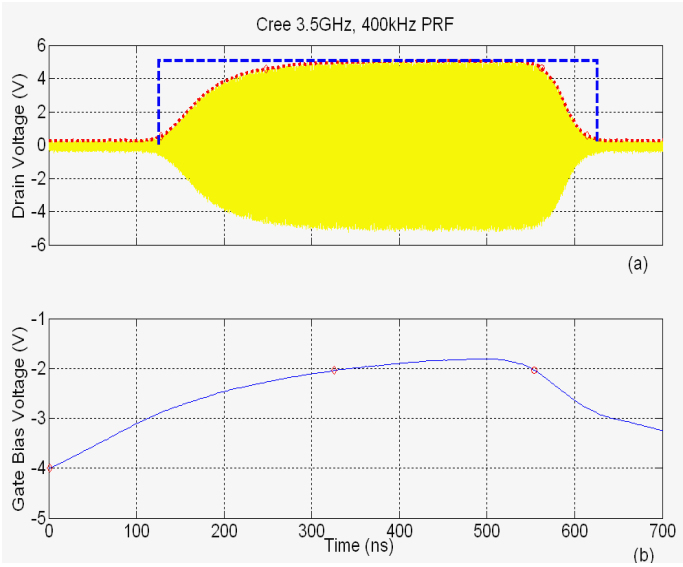

Fig 8 (a) Drain output at 9 dBm input power and 400 kHz PRF, Envelope (dotted), Ideal Envelope (dashed) – (b) Gate Bias

IV. Future Work

Future work will focus on repeating the experiments presented in this paper at much higher power levels and on devices with higher power ratings.

Bare die devices will also be subjected to similar tests at frequencies ranging from 6 to 10 GHz and PRFs up to 600 kHz.

Modifications to the bias switching circuit are currently being designed to improve rise and fall times.

V. Conclusions

In this study the suitability of commercially available GaN samples to pulsed operation has been demonstrated. The devices presented a consistent and reproducible performance at specific power levels across a broad range of Pulse Repetition Frequencies (PRFs). These devices could find application in S-band radars which utilise much lower PRFs than those analysed in this study.

The reason for pushing the devices to higher PRFs was to analyse the response that their structure would have to repetition frequencies which are used at higher RF frequencies. Seeing that higher frequency devices will maintain some commonalities with their lower frequency counterparts, this gives some degree of confidence that future devices could be utilised for pulsed RF applications which operate in higher frequency bands.

Acknowledgment

The authors wish to thank Cree Inc and Novacom Microwave for supplying free samples and providing great assistance and support.

Also a special thanks goes to our lab technician Mr Ken Stevens for all his help with the design and setup of the experiments.

This work has been partially supported by MBDA.

References

[1] Jardndal, A.H., Large Signal Modelling of GaN Device for High Power Amplifier DEsign. 2007, University of Kassel: Kassel.

[2] Vetury, R., et al., The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs. IEEE Transactions on Electron Devices, 2001. 48(3): p. 560-566.

[3] Meneghesso, G., et al., Surface-related drain current dispersion effects in AlGaN-GaNHEMTs. Ieee Transactions on Electron Devices, 2004. 51(10): p. 1554-1561.

[4] Binari, S.C., et al., Trapping effects and microwave power performance in AlGaN/GaN HEMTs. IEEE Transactions on Electron Devices, 2001. 48(3): p. 465-471.

[5] Trew, R.J. Wide bandgap transistor amplifiers for improved performance microwave power and radar applications. in 15th International Conference on Microwaves, Radar and Wireless Communications, MIKON - 2004, May 17-19 2004. 2004. Warszawa, Poland: Institute of Electrical and Electronics Engineers Inc., New York, NY 10016-5997, United States.

[6] Okamoto, Y., et al., Improved power performance for a recessed-gate AlGaN-GaN heterojunction FET with a field-modulating plate. IEEE Transactions on Microwave Theory and Techniques, 2004. 52(11): p. 2536-2540.

[7] Karmalkar, S. and U.K. Mishra, Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate. IEEE Transactions on Electron Devices, 2001. 48(8): p. 1515-1521.

[8] Wu, Y.-F., et al. Field-plated GaN HEMTs and amplifiers. in 2005 IEEE Compound Semiconductor Integrated Circuit Symposium, CSIC, Oct 30-Nov 2 2005. 2005. Palm Springs, CA, United States: Institute of Electrical and Electronics Engineers Inc., New York, NY 10016-5997, United States.

[9] Moon, J.S., et al., Gate-recessed AlGaN-GaN HEMTs for high-performance millimeter-wave applications. IEEE Electron Device Letters, 2005. 26(6): p. 348-350.

[10] Ando, Y., et al. Novel AlGaN/GaN dual-field-plate FET with high gain, increased linearity and stability. in IEEE International Electron Devices Meeting, 2005 IEDM, Dec 5-7 2005. 2005. Washington, DC, MD, United States: Institute of Electrical and Electronics Engineers Inc., Piscataway, NJ 08855-1331, United States.